

## Technical Approach Document

For Google Little Box Challenge project By Helios team

In this Google Little Box Challenge project, Helios team has developed a key Intellectual Property (IP) of driving high voltage Field Effect Transistors (FETs) with isolation in a very innovative way to optimize the system switching performance. As the result, the driving circuits become very simple and overhead power consumption becomes very minimal. It leads to very simple power generation circuits necessary to power all the isolated FET drivers on top of superior driving performance. Besides, it improves isolation between low voltage control circuits and high voltage power circuits, which makes the development and debugging efforts much easier and much less chance to blow-up circuits due to control code errors and any other handling errors during debugging.

Another key IP Helios team invented in this project is the power filtering technologies, which enables us to handle large current with much smaller passive components resulting in significantly smaller physical sizes of power filters. Most importantly, the advanced and simple architecture we invented enables us to have the shorted path from DC input to AC output and least amount of components in the middle.

Intellectual properties and technologies developed for this project can have broad range of applications in various industries, besides solar inverters. For example, high power density high efficiency AC-DC converters, small size high power AC adapters, light weight small size high efficient on-board electrical vehicle chargers etc.

Among above mentioned technologies, isolated FET driving technology can be used to replace current iso-drivers in FET or IGBT driver IC market. Iso-drivers in today's market all require a separate isolated DC voltage, although small power in tens to hundreds of milliwatt range, no matter their isolation barrier is implemented by using opto, or transformer, or capacitors. This technology can become a large market itself.

Based on above and many other innovations, Helios team has created a two-segment topology to convert DC input into AC output power with power density as high as 269W per cubic inch. Its high level schematic is shown in figure 1 below:

This schematic is implemented in a little box sized as small as 4.15 inch x 1.60 inch x 1.12 inch < 7.5 cubic inch. It translates into the power density of 269 watt per cubic inch. In this converter, following key performances are achieved:

**1. 120 Hz input current/voltage ripple requirement** are implemented by adding a power buffering stage at the input side of the inverter, which transferring whatever input voltage level into a steady intermediate DC voltage. The intermediate DC voltage serves as a buffer to absorb the input current/voltage variation and maintain relatively smaller 120Hz input current and voltage ripple, so the 120Hz input current and voltage ripple requirements are met.

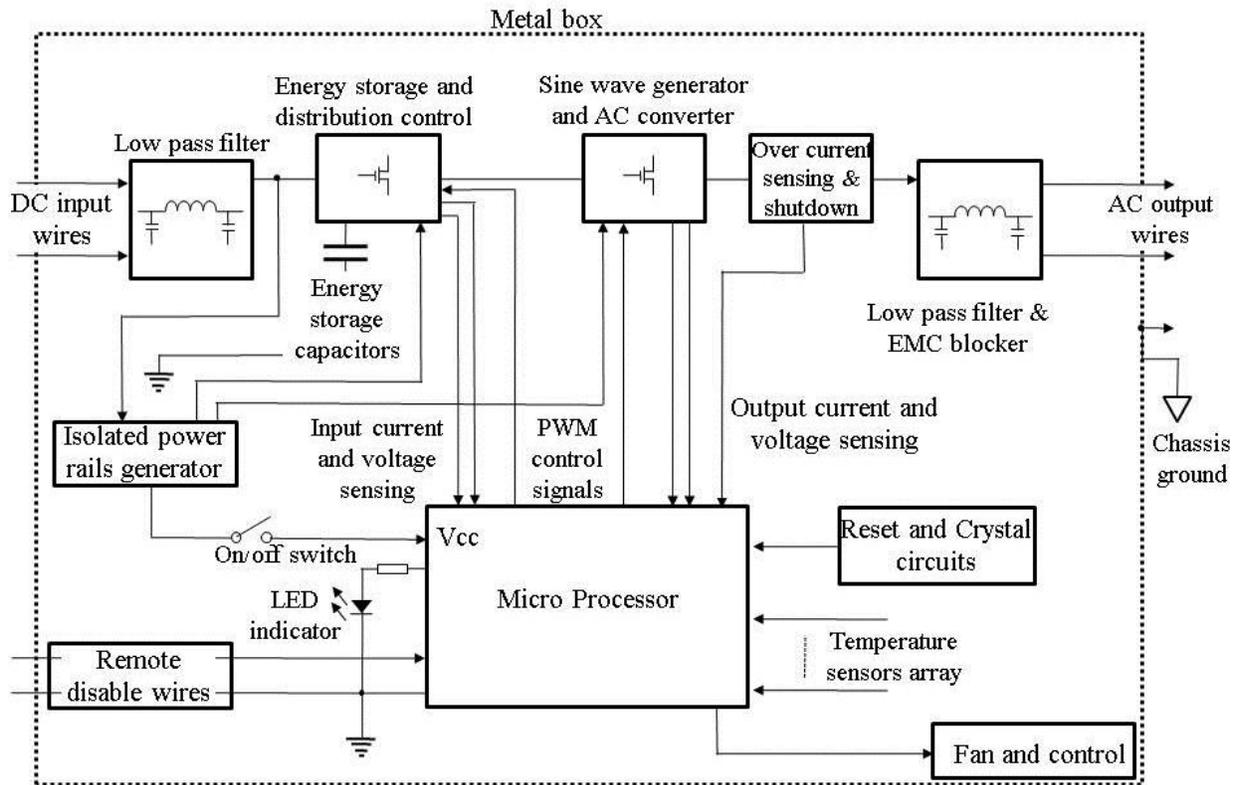


Figure 1. High level schematics of Helios DC-AC converter

The absorbed energy is stored in a capacitor bank. When the output voltage is at the low portion of sine wave, and the corresponding input current is low, the system controller absorbs extra current into the capacitor bank to maintain the same level of input current. When the output voltage is at the high portion of output sine wave, the energy in the capacitor bank is outputted to supplement extra input current needs of the high portion of AC output. By controlling the amount of energy stored in the capacitor bank in an innovative way, much smaller capacitance and much smaller ripple current are required than conventional solutions. Therefore, much smaller system volume is required, and higher power density is realized. The amount of capacitance used in the capacitor bank of the converter is at the range of hundreds micro Farad.

**2. Miniaturization of components for DC-AC conversion:** Since the largest size components in this DC-AC inverter are passive filters, meaning inductors and capacitors, Helios team has invented a new IP technology to construct those filters with smaller passive components to reach smaller overall size. Helios team has also invented a technology called Time Division Components Multiplexing (TDCM). This technology allows multiple circuit segments to share bulky passive components at the different timing to significantly reduce the overall system size. At the same time, Helios team uses high power Silicon MOSFETs creatively by utilizing high voltage switching at low current and high current switching at low voltage with increased switching frequency of Pulse Width Modulation (PWM) control signals. All above technologies help to decrease the sizes of passive filters required for smoothing square wave pulses into a sine wave with minimal harmonic distortion.

Comparing with the traditional methods of simply increasing switching frequencies of inverting a fixed voltage DC input into AC output, the Helios way is another group of key IPs developed for this project. The smaller passive component sizes translate into higher power density.

Additionally, some advanced wiring materials are used in inductors to reduce their DC resistance. Such improvement in the passive components themselves helps improving energy efficiency and cutting thermal generations at the same time. It further increases the power density of this inverter.

**3. Thermal management** is one of the major challenges of this project. Helios team resolves this challenge mainly through overall inverter system power efficiency improvement. The higher overall system power efficiency results in reduced amount of waste heat generation and lessens the pressure on thermal management.

We carefully design our inverter circuit and select components to minimize their DC resistance and carefully design switching mechanism to minimize switching losses, so that we have minimum amount of waste heat to be dissipated. Our DC-AC conversion efficiency is greater than 97.8% at full load of 2 KVA. Therefore, we have only 44 Watts of heat which must be dissipated in order to prevent an unacceptable temperature rise.

We developed a special surface treatment method to increase the surface heat exchange efficiency between our internal heat generation devices and the box case material, and the heat exchange between our box case external surfaces to environment air. Additionally, since our box size is small, we do not rely on surface area of our little box to dissipate heat. We do not rely on the higher operation temperature of our switching devices to relaxing the local thermal management requirements either. Instead, we use high air flow fans to generate forced airflow and specially designed air channels inside and outside the little box to dissipate the maximum amount of waste heat. In this way, we keep all the heat generating components, including switching devices, filtering devices, and current conducting devices, to work at the lowest possible temperature. Under such conditions, those components all have lower DC resistance, it in turn further reduces the heat generation and improves system efficiency, and eases thermal management problem, and enables higher power density of the inverter.

Furthermore, some advanced thin thermal conducting materials are used to reduce thermal resistance and provide electrical isolation. Such improvement in the thermal materials helps improving thermal conductivity and cutting sizes thermal materials occupy at the same time. It further increases the power density of this inverter. As a result, we avoid the presence of hot spots above 60° C.

**4. Electromagnetic Compliance (EMC)** becomes possible mainly due to our spread spectrum design of our switching circuits and their control signals and system control algorithms, even they are all high frequencies at hundreds KHz ranges. Besides, innovative methods of EMC filtering, blocking and shielding successfully help to limit both conducted and radiated electromagnetic interference within acceptable levels for FCC Part 15 B compliance. Very importantly, the way of

our circuit board design significantly reduces EMC through smaller form factor of our carefully selected components, shortest possible connection lengths between components, especially key high power switching components, offers both less EMC and minimum system volume simultaneously. As the end result, our inverter passes both conducted and radiated EMC.

### **Safety and protection circuits**

In our system, both input and output over current and over voltage protection are implemented in hardware. Micro second reaction time becomes possible. In slow reaction mode, protections are slowed down by firmware to match the requirements. Since temperature change is relatively slow, our over temperature protection is implemented in firmware completely, by monitoring temperatures through multiple temperature sensors across the different parts of the circuit, devices and surfaces.

### **Appendix:**

- Design team

**Jack Zhu** immigrated to the United States in 1993 and has received his Ph.D degree in Electrical Engineering from the University of Maryland in 1999.

Dr. Zhu joined Bell Labs in 1996 and has successfully developed several products there from DSP (Digital Signal Processor) based feature telephones and digital answering machines, to indoor cell phones, wired and wireless optical telecommunication systems, and power supply systems, etc. He holds three US patents and one European Union Patent.

Dr. Zhu has been principal investigator for two National Science Foundation projects and two Department of Defense research projects. He has designed and developed many products in solar systems, power inverters, power supplies for computer and industrial control systems. From above experience, he developed strong expertise on power system architecture, thermal management, EMC compliance etc.

**Mari Y. Ma** received her Master and Ph.D degrees in Electrical and Computer Engineering from the University of Maryland at College Park in 1998 and 2004 respectively.

Dr. Ma is currently a chief firmware architect and firmware design engineer. She joined Bell Labs in 1998 and has designed firmware for multiple products including DSP based feature telephone and digital answering machines, MEMS (Micro Electro Mechanical Systems) based optical communications, power supply devices etc.

Dr. Ma has been co-Principal Investigator for two National Science Foundation funded research projects and two US Air Force funded research projects. She is the main firmware architect of above research projects and has designed firmware for multiple products ranging from AC-DC power supplies, to solar power inverters, and to DC-DC power supplies for computer CPU chip sets etc. Her expertise includes high efficient power converter control algorithms design, high efficient control firmware design and programming and firmware related project management.