

Technical Approach Document.

Team name: LBC Slovakia

Registration code: 545-40NdCL-56238

- Power density: 130W/in³
- Switch level schematic:

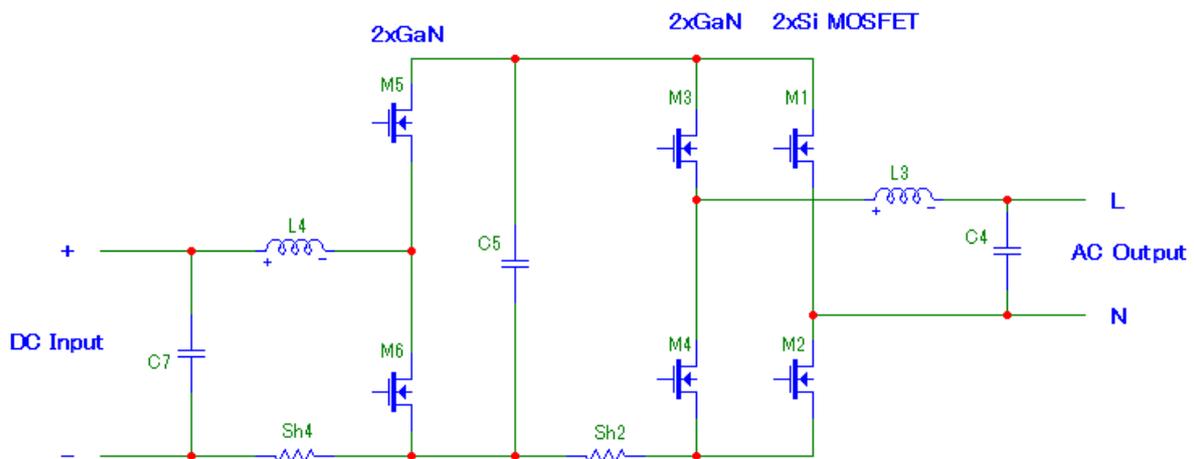


Fig.1 Switch level schematic.

- **Order of magnitude passive components values:**
Energy storage element C5 is aluminum electrolytic capacitor with capacitance of under 500 μ F.
Boost inductor L4 and inverter filter inductor L3 are ferrite core and litz-wire winding inductors, inductance is of around 100 μ H.
- **Order of magnitude frequency values:**
Boost stage (M5, M6) has switching frequency below 150 kHz
Fast inverter leg (M3, M4) has switching frequency below 150 kHz
Slow inverter leg (M1, M2) is switching at 60 Hz
- **Semiconductor device type:**
In the boost stage and one leg of the inverter bridge there are used E-mode GaN FETs. The AC frequency leg of the inverter is equipped with super junction Si FETs.
- **DC input and AC output sides are equipped with EMI filters** based on multi stage LC cascades. Inductors are made of high performance ferrites, alloy powder and nanocrystalline materials, capacitors are made of high performance ceramics.

120Hz input current and/voltage requirements:

120Hz ripple requirements are met by employment of active power factor correction (PFC) boost stage which is controlled by innovative algorithm in voltage mode for maximum dynamic stability. Digital signal processor (DSP) generates drive signals for the boost switches and manages the AC ripple on the DC input while the bulk filter capacitor works like reactive energy storage element and experiences high AC ripple voltage instead.

The higher the AC ripple voltage on the bulk filter capacitor is, the higher utilization of this capacitor can be. Very high ripple of the capacitor voltage enables to use very small size capacitor. Actually, 4 times smaller capacitor is used in the active PFC solution in comparison to passive solution when only bulk filter capacitor (without active PFC stage) would be used. Overall volume of the active ripple steering stage is still more than 2 times smaller than the volume of simple capacitor in passive filtering solution. Moreover, with the active ripple steering solution, the voltage/current ripple on the DC input can be substantially more reduced than with reasonably big capacitor in passive solution.

As the overall solution volume includes the cooling system of the semiconductor switches, very fast switches and moderate switching frequency is used. This gives low losses and small heatsink even at hard switching of the stage.

Miniaturization of components for DC-AC conversion:

The most compact solution is based on tradeoff between power losses, noise emissions and output parameters quality. This solution employs simple but high performance topology of full bridge with very fast switches and multi stage EMC filter.

The switching frequency is chosen low enough to keep low switching losses and high enough to keep small EMI filter. The switching frequency is chosen below the EMC band defined by FCC standard. This enables to reduce the EMI filter even more as only higher harmonics of the switching frequency must be attenuated below FCC limits. The EMC filter is split to more stages what results in smaller overall filter.

The switches are GaN E-mode FETs, its power losses are very low even at hard switching, so the heatsink can be very compact. Drive losses are substantially smaller than at silicon switches as well.

The inverter topology is driven by high performance DSP controller in voltage mode what gives high dynamic stability, high quality of output parameters even at no need to use any bulk sensors for reliable operation.

Neither multi-phase interleaved topology nor special measures for switching losses reduction (soft switching) are applied as the simple solution resulted in the least overall volume.

Thermal management:

Successful thermal management is based on generation of least losses in components, on increase of cooling area by split heat generating parts into more pieces of smaller parts and on properly designed layout for highly efficient sinking of the heat by forced flowing air. The air flow is focused to flow through/along the most heat generating parts.

For least power loss generation in semiconductor switches, the high performance devices like E-mode GaN FETs and super junction FETs are used. In addition, all power parts related to the switches (inductors, pcb layout) are optimized to eliminate the increase of parasitic capacitances which could increase switching loss in the switches even to provide paths for noise propagation. Regarding the power inductors, loss reduction is reached by utilization of high performance ferrite materials and stranded wire windings with special winding style.

For best cooling of the inductors the special shapes with high surface to volume ratio are chosen. No hot part inside the box is actively cooled to the box wall so the box surface can be kept cool (<60°C). Air flow of the fan is dimensioned and directed to keep the air temperature below 60°C, this keeps the temperature of the box walls under limit. Properly chosen dimensions (its proportions) of the box supports this as well.

Electromagnetic compliance:

The EMC compliance of the solution is based on elimination of sources of the noise, on elimination of paths which the noise is propagated through and on maximization of the ratio of damping factor to size of the filter. As the filter contributes to the power losses and to volume as well, most care must be taken of the noise sources and noise paths elimination.

Firstly, the switches are driven within specific dV/dt and dI/dt to reduce bandwidth and magnitude of the noise generated. As the EMC compliance standard defines the lower limit of tested frequency band, the fundamental switching frequency was chosen below this limit and the filter was dimensioned for higher harmonics of the switching noise then only. As the harmonics of the noise drop in magnitude with order of the frequency, the filter can be more compact to meet the FCC limits.

Secondly, the parasitic elements of the circuitry, inductances of loops, capacitances of junctions (spots), inter-winding and inter-layer capacitances are reduced as much as possible by properly designed layout of the pcb and winded parts (inductors). Faraday shielding is used to eliminate the propagation of electric field from noisy spots. Topology of the filter and its properly chosen layout supports the performance of the overall solution.

Thirdly, the filter is split to multi stage solution, 4th order filter on DC input side and 6th order filter on AC output side. Performance of the filter was calculated in more iterations for various options (number of stages, its proportions), the least size solution with required attenuation was chosen.

Biographical information appendix:

Martin Pietka (team's point of contact) was born in Ilava, Slovakia, in 1983. He received master degree from University of Zilina, Slovakia, in 2007. He has been working as software engineer.

He is software engineer in "LBC Slovakia" team.

Andrej Tereň was born in Detva, Slovakia, in 1978. He received master degree in power electronics from University of Zilina, Slovakia, in 2001.

Since that he was joining companies developing UPS, telecom frontends and rectifiers. His work is focused to lossless switching topologies, thermal management, layout optimization for EMI/EMC performance and novel technologies implementation in switch mode power supplies. Currently he is working on development of industrial and transportation power supplies for industrial and transportation/automotive market.

He is joining the "LBC Slovakia" team as hardware engineer.

Lubos Drozd was born in Ilava, Slovakia, 1981. In 2005 he received master degree from Slovak University of Technology in Trnava, Slovakia. Since this time, he has been working as mechanical design engineer in automotive industry and power electronics.

He is mechanical designer in "LBC Slovakia" team.

Marian Vranka was born in Ilava, Slovakia, 1977. In 2001 he received master degree from Slovak University of Technology in Bratislava, Slovakia. Since this time, he has been working as electrical design engineer with focus on power electronic.

He functions as hardware engineer in "LBC Slovakia" team.

Peter Sedlacko was born in Zilina, Slovakia, in 1971. He received master degree in power electronics from Military Academy in Liptovsky Mikulas, Faculty of Technical Cybernetics, Slovakia, in 1996.

Since that he was joining companies developing hardware for telecom communications devices, frontends and rectifiers. His work is focused to lossless switching topologies, thermal management, layout optimization for EMI/EMC performance and novel technologies implementation in switch mode power supplies. Currently he is working on development of industrial communications systems for industrial market.

He is joining the "LBC Slovakia" team as hardware engineer.