Technical Approach

Team Name: !verter	**Registration Code:** 545-Xw08K5-56618

1. Overview

In this document, the general approach and important details of the proposed inverter system, which meets the full (initial) specifications, i.e. the 5 mA ground current limit and the DC input current ripple criterion at all requested power factors of the load (0.7 – 1), are described. The total volume of the system is 14.22 in^3 resulting in a power density of 140.60 W/in^3.

The topology of the system is depicted in Fig. 1. This topology and the corresponding values of the passive components are the result of a comprehensive multi-objective design optimization process which considers loss and volume models of semiconductors, passive components and measurement/control circuits, the performance of cooling systems, and the given constraints of the LBC specifications.

The inverter stage of the system consists of two output phases, each of which is formed by two interleaved bridge leg stages in buck-configuration. Each of the four bridge legs is operated with an advanced triangular current mode (TCM) modulation scheme [1,2] controlled with an FPGA, whereby the (variable) switching frequency is in the range of 100s of kilohertz. The orders of magnitude of all relevant passive components is provided in Tab. I. New Normally-Off gallium nitride (GaN) Gate Injection transistors, which are driven by a novel high-performance gate driver [3], are used for implementing the four bridge legs. In Section 2, the DC link energy storage approach is described in more detail. Thereafter, an overview on approaches used to minimize the volume of the passive components is given in Section 3. Subsequently, the thermal management and cooling concept is presented in Section 4. In Section 5, an overview on the EMI filter is given. Finally, an outlook relating to the recent modifications of the LBC specifications which will allow the realization of a different inverter concept [4] with higher power density is given in Section 6.

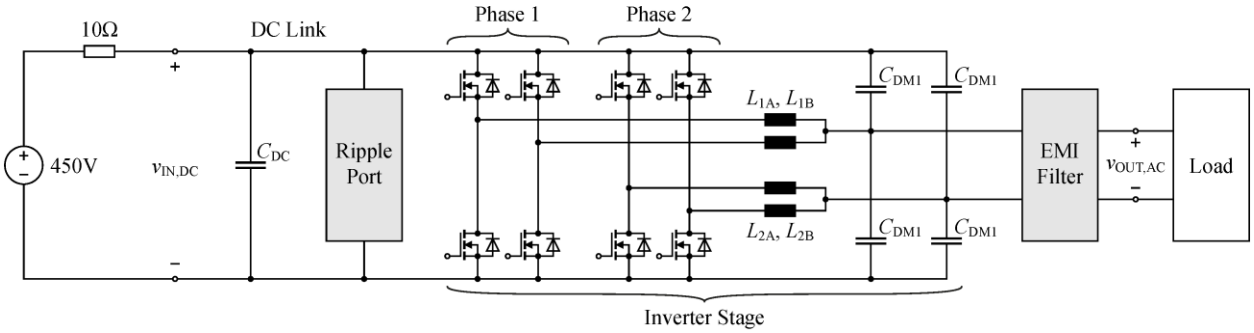

Fig. 1. Topology of the presented inverter consisting of two output phases, each of which is formed by two interleaved bridge legs in buck-configuration. The system DC-side energy storage (Ripple Port) is detailed in Fig. 2 and the EMI filter is presented in Fig. 4.

2. 120 Hz DC Input Current/Voltage Ripple Requirements

In case an electrolytic bulk capacitor would be used for meeting the input current/voltage ripple criteria, a large capacitance value of at least 1.9mF (according to the

initial specifications) would be needed, which would result in a large volume of the DC energy storage. This is the case because the energy pulsations of the bulk capacitor, which are caused by the AC component of the sinusoidal power pulsation drawn by the load at twice the output frequency (120 Hz), are only marginal compared to the total capacitor's stored energy, i.e. due to the low allowed DC link voltage variation the capacitor basically remains fully charged and/or its energy storage capacity is hardly utilized.

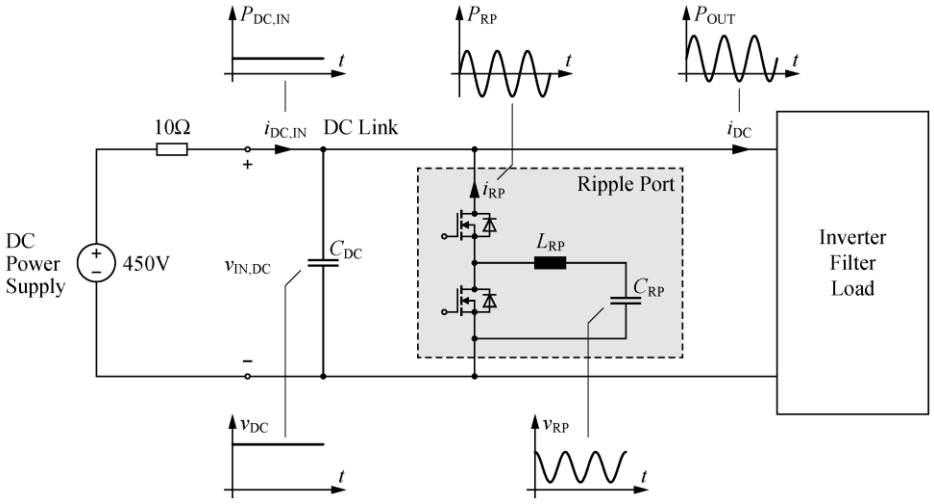

Fig. 2. Topology of the employed Ripple Port including schematic visualization of power flows and capacitor voltages.

In order to minimize the capacitance and volume requirement of the DC energy storage, in the proposed system the 120Hz DC current/voltage ripple component is minimized by a state-of-the-art active buck-type Ripple Port (RP) (cf. Fig. 2) utilizing a new control scheme [5]. The RP largely compensates the AC component of the sinusoidal power pulsation drawn by the load. The RP unit stores/recovers the energy contained in the power pulsations in/from a capacitor C_{RP} which is, in contrast to a standard electrolytic storage capacitor in the DC link, (dis-)charged to a significant extent, i.e. shows a large voltage ripple. Accordingly, a much smaller capacitance value is required which allows to reduce the total volume of the DC link energy storage even though additional semiconductors, an inductor L_{RP} and auxiliary circuits are needed. In order to meet the high RMS-current requirement and energy storage capacity at minimal volume, a novel ceramic capacitor technology is used for C_{RP} which provides 100s of microfarads in highly compact form. C_{DC} is only needed for filtering switching frequency pulsations and consists of ceramic capacitors in the range of several microfarads. The semiconductors, the type of inductor L_{RP} and the type of modulation (TCM) are identical to the inverter stage. L_{RP} provides several microhenries.

3. Miniaturization of Components for DC-AC and DC-DC conversion

Different approaches are used to minimize the volume of the passive components, i.e. the power inductors and the output capacitors, which are employed in the inverter stage and the RP, as described in the following:

- The values of the passive components are reduced by selecting a high switching frequency in the range of 100s of kilohertz which is, however, only enabled by selecting a new type of Normally-Off GaN Gate Injection transistor and a newly

developed high-performance gate driver [3], in combination with using a TCM modulation scheme [1,2] promoting zero voltage switching and resonant switching transitions, i.e. comparably low switching losses.

- The values of the output capacitors C_{DM1}, cf. Fig. 1, could be reduced significantly by using two interleaved bridge legs per output phase, whereby the high-frequency current ripples are compensating each other to some extent and the resulting frequency of the remaining current ripple is doubled compared to the individual bridge leg switching frequency.
- The volume of the inductors could be minimized by developing a novel type of multiple air gap foil winding inductor with extremely thin isolation layers [6,7].
- The volume of the DC link capacitor C_{DC} could be minimized by using a novel and highly compact type of ceramic capacitor.

4. Thermal Management

In order to extract the heat generated by the inverter and the RP, which is in the range of several tens of Watts, a heat management approach based on natural convection and forced air cooling is applied. For the given converter volume the surface area, which provides heat exchange to the ambient by natural convection, is maximized by designing a very flat and long shaped system considering the height constraints of the passive components (capacitors, inductors). In order to avoid means and consequently volume for conducting the heat to a central cooling unit and/or isolating hot parts from the enclosure, a distributed forced air cooling system, which consists of ultra-flat blowers and high fin number copper heat sinks, was designed, cf. Fig. 3, and optimized towards a cooling system performance index, *CSPI* (heat conductivity per volume [8] of 100s of Milliwatts per cubic inch Kelvin; i.e. a factor of >5 higher in performance than commercial heat sinks.

Fig. 3. Cooling system unit consisting of ultra-flat blowers and high fin number copper heat sinks; two cooling units are placed on opposite upright/vertical faces of the system.

5. Electromagnetic Compliance (EMC)

The topology, the modulation and the resonant transition switching of the proposed system, cf. Fig. 1, promotes an EMI filter of low volume. On the one hand, for the generation of the AC output voltage the two phase output voltages are actively controlled to values directly symmetric around half the DC-link voltage $v_{IN,DC}$, i.e. (ideally) no low-frequency common-mode (CM) component of the generated AC output voltage occurs. In addition, the switching commands of the two output phases are synchronized 180° out of phase with each other which results in a (partial) cancellation of the CM voltage at

the switching frequency. Nevertheless, a CM inductor is used in the AC side EMI filter stages for filtering remaining switching frequency components. The stray inductance of the CM inductor contributes to the differential-mode (DM) filter inductors. On the other hand, the high but variable switching frequency in the range of 100s of kilohertz enables to select a high corner frequency of the CM and/or DM filter stages. After an overall optimization (considering also the higher switching losses at higher frequencies), the minimum volume of the EMI filter was attained by selecting a two-stage topology, cf. Fig. 4, with the values given in Tab. I.

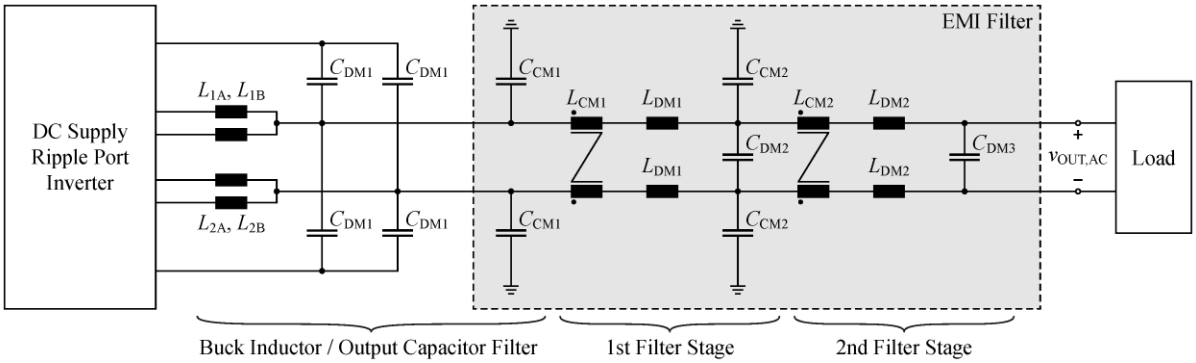

Fig. 4. Topology of the EMI filter consisting of two CM/DM filter stages.

Tab I. Orders of magnitude of the EMI filter's passive component values.

Components	Value	Unit
L_{1A}, L_{1B}, L_{2A}, L_{2B}, L_{DM1}, L_{DM2}	1s of	microhenries
L_{CM1}, L_{CM2}	100s of	microhenries
C_{DM1}, C_{DM2}, C_{DM3}	1s of	microfarads
C_{CM1}, C_{CM2}	10s of	nanofarads

6. Outlook

Due to the recent change of the specifications on June 25, 2015, both the inverter topology and the EMI filter will be modified [4] in order to further improve the power density of the inverter. As proposed in the LBC Q&A document, a more detailed description is given in the appendix of the technical application document.

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[6] F. Zajc, "Flat band winding for an inductor core," United States Patent Application pending.

[7] F. Zajc, "Multi gap inductor core, multi gap inductor, transformer and corresponding manufacturing method," European Patent No. EP 2 528 069 B1, granted Dec. 18, 2013.

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Eckart Hoene was born 1970 and studied electrical engineering at the Technical University Berlin. After finishing he joined the Fraunhofer IZM in 1997 as scientific assistant and worked towards his PhD EMI of electrical drive systems, which was granted in 2000 by the Technical University Berlin. He continued at Fraunhofer as Postdoc, group leader, business development manager. Since 2014 he additionally is Adjunct Professor at Aalborg University, Denmark. His main topics are packaging for power electronics, inverter design and electromagnetic compatibility.

Johann W. Kolar is a Fellow of the IEEE and received his M.Sc. and Ph.D. degree (summa cum laude) from the University of Technology Vienna, Austria. He is currently a Full Professor and the Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. Dr. Kolar has proposed numerous novel PWM converter topologies, and modulation and control concepts, and has published over 650 scientific papers in international journals and conference proceedings and has filed more than 110 patents. He received 21 IEEE Transactions and Conference Prize Paper Awards, the 2014 Semikron Innovation Award, the 2014 IEEE Middlebrook Award, and the ETH Zurich Golden Owl Award for excellence in teaching. The focus of his current research is on ultra-compact and ultra-efficient converter topologies employing latest power semiconductor technology (SiC and GaN), wireless power transfer, Solid-State Transformers, Power Supplies on Chip, and ultra-high speed and bearingless motors.

Dominik Bortis received the M.Sc. degree in electrical engineering and Ph.D. degrees from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008. During his studies, he majored in communication technology and automatic control engineering. After the internship with ABB Switzerland, Turgi, he worked during his diploma thesis with the company Levitronix. Since 2008, he has been a Postdoctoral Fellow with the Power Electronic Systems Laboratory, ETH Zurich. In 2010, he founded the company Enertronics GmbH, Zurich, Switzerland, which is a consulting company for power electronics system engineering and prototyping.

Yanick Lobsiger received the B.Sc. and M.Sc. degrees in electrical engineering and information technology from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2007 and 2009, respectively. In spring 2015, he received the Ph.D. degree from the Power Electronic Systems Laboratory, ETH Zurich, Switzerland, where his research focus was on novel closed-loop IGBT gate drive concepts. He is currently working as a postdoctoral researcher at the same laboratory.

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Stefan Hoffmann was born in Muehlhausen, Germany in 1972. He successfully completed his master's degree at the Technical University Berlin, Germany in 2010. His main focus was power electronics and electrical drive engineering. At the beginning of 2011 he was assigned as a research assistant to the Power Electronics working group at Fraunhofer institute IZM. He is currently working on prototype development, passive components and EMC in the power electronic area.

Adam Kuczmik was born in Berlin, Germany in 1986. From 2006 he studied computer engineering. His main focus was microcomputer systems and power electronic. He obtained his master's degree in 2013 at the Technical University Berlin, Germany. Since then, he has been employed as a research assistant in the power electronic group at the Technical University Berlin/Fraunhofer institute IZM. Momentarily, he is working on controlling of power converter systems.

Oleg Zeiter was born 1983 and successfully completed a master's degree in power and automation electronics. Since 2012 he was assigned as a research assistant to the Power Electronics working group at Fraunhofer institute IZM in Berlin. He is currently working on prototype design and system development of high frequency power converters and driver electronics for high density power applications.

Franc Zajc born in 1952 is an independent inventor since 1970 working in Slovenia. By 1985 he worked for Iskra Slovenia on measuring methods for Si power diodes. In 1985 he launched his own research on electric motors, which resulted in a multiphase and multipole machine invention. From year 2000 on his work in power electronics on reducing the switching and conversion losses continues. His research on fields of Near Zero Interlock Delay (NZID) driving principle and High-Q multi gap inductor makes it possible to significantly increase the switching frequency in power conversion.