

# CZARS inverter architecture

## Controllably Zero input ripple Auxiliary Resonant Simplified architecture inverter

We present a novel and compact inverter architecture, comprising only seven primary switches and utilizing a novel PWM subcarrier and control algorithm to achieve controllably zero input ripple current. An auxiliary resonant ZVS (zero voltage switching) circuit reduces switching loss to allow a high primary PWM frequency. An energy recovery circuit recovers switching energy in the auxiliary ZVS switch itself, to power the TI Piccolo DSP, fans and other ancillaries.

### CZARS Architecture highlights

- 149W per cubic inch with novel 7 switch, 2 inductor architecture
- 97% efficiency
- GaNSystems GaNFET switches with >500kHz primary PWM carrier frequency
- Single auxiliary resonant commutated ZVS dual switching pole
- 450V – 200V wide swing, 5 Joule, TDK CeraLink energy storage capacitor bank
- Storage capacitor charging using novel 25kHz secondary PWM sub-carrier
- Input isolation during capacitor connection phase – Low EMI
- Symmetrical operation: no line frequency component is impressed on the DC input
- High magnetics utilization – compact magnetics

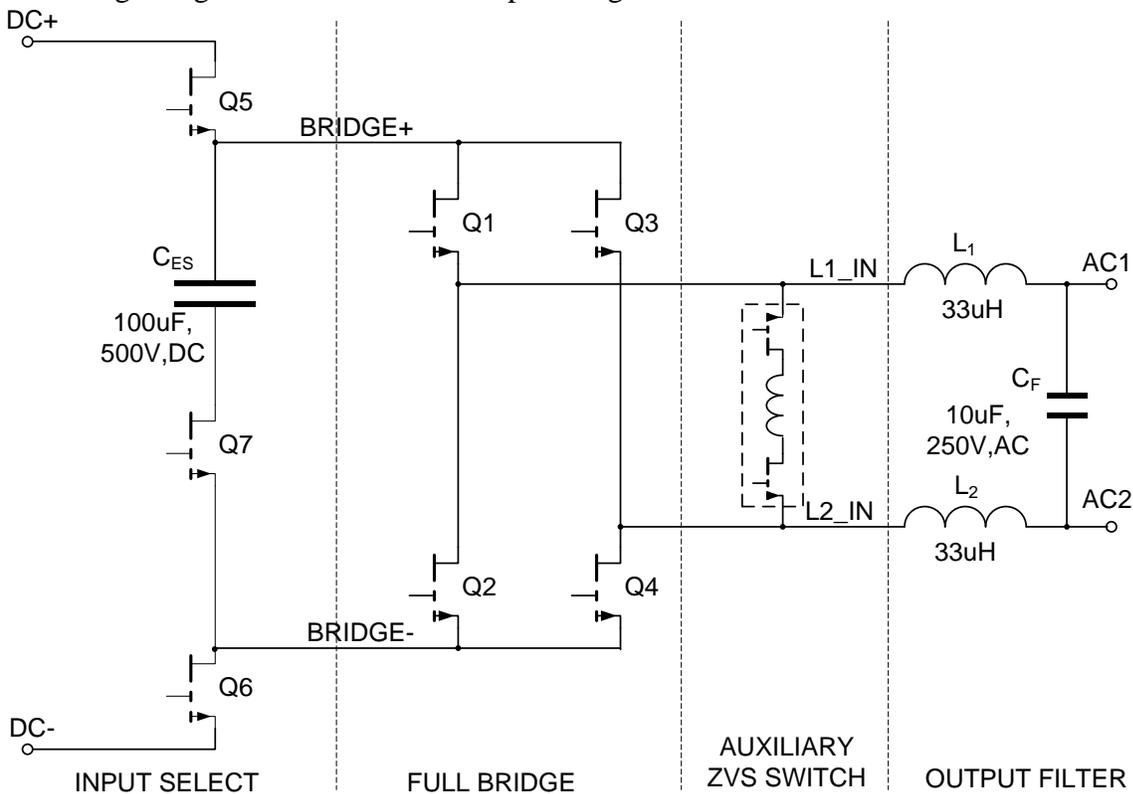


Figure 1

## Architecture overview

The CZARS architecture is based on a conventional full-bridge PWM switch followed by a conventional LC output filter. To this basic circuit, three additional circuit elements have been added:-

1. 5.3 Joule, 450V energy storage capacitor.
2. Input select stage.
3. Auxiliary resonant ZVS switch.

The input select stage connects the full-bridge rails to either the DC input or to the storage capacitor. When the capacitor is selected, the DC input is isolated and vice versa. The energy storage capacitor is operated in a deep charge/discharge cycle. The auxiliary ZVS switch facilitates the symmetrical commutation of the split phase switching pole with very low energy loss and allows a high PWM frequency; the high PWM frequency in turn allows a reduction in the size/volume of the passive components.

## 120Hz input current/voltage ripple

The energy storage capacitor is not directly connected to the DC input supply. It is charged or discharged at a rate determined by a control loop regulating the input current to a constant value determined by monitoring the AC output power. The input ripple is therefore controllably zero, though in practice displays 120Hz ripple due to finite loop gain and the fact that the energy storage capacitance has been minimised for the purposes of the competition. At full load, the CZARS inverter is able to cycle the energy storage capacitor over a 200V to 400V range leading to very high utilization of the capacitor's available energy storage capability.

## Miniaturization of components

The energy storage required for ripple reduction is fixed by the application at ~5J for 60Hz, so the approach to miniaturization was to choose the highest energy density available. Using two physically interleaved banks of 5uF, 500V TDK CeraLink modules, the required energy storage takes a volume of <math>2.5 \text{ in}^3</math>.

The inductor volume has been minimized by the development of an entirely novel architecture and algorithm requiring only a single pair of inductors to mediate all energy transactions in a very efficient manner. At full load, these inductors are used near to their saturation current limit throughout a large percentage of the line frequency cycle, meaning the magnetics utilization is very high and the overall volume is very low.

To be able to use inductors of a compact size, a high switching frequency is needed. To enable this we first selected GaNSystems power devices as having exceptionally low parasitic loss in relation to their low 'on' resistance. Because the proposed switch architecture is ideally structured to take advantage of Auxiliary Resonant Commutated Pole ZVS switching, with very modest additional component count, we were able to further reduce the main switching loss by a factor of four. Then by recovering ~50% of the auxiliary circuit residual switching loss to power the DSP, fans and auxiliary circuits, the main switching energy loss is effectively reduced again by a further factor of two. All high voltage pump and energy recovery circuits use Cree SiC Schottky diodes to minimise diode loss. The very low overall switching loss enables the use of a primary switching frequency in the range 500-1000kHz and the use of compact inductors.

## Thermal Management

At such a small size fans were unavoidable to increase air flow. To maximize the efficiency of the fans it was important to have a fan intake duct/chamber to align the air flow with the blades. The fans have been configured to blow air out of the box to allow an internal chamber that could be partially shared with other components and functions. By careful positioning of internal components the plenum chamber is partly formed from airflow space between the coil and ferrite of the inductors and partly formed by the spaces between a dense array of copper cooling fins integrated with the structure of the enclosure. The fans are positioned to cause entrainment of secondary airflow along cooling fins milled into an external face of the enclosure. The GaNFET 'on' resistance increases markedly with temperature, which makes it doubly important to equalize the temperature around the enclosure. To this end the enclosure is made of copper in two parts. The main part is machined from a copper billet and then folded into shape allowing careful thickness profiling and optimal use of any available internal space either for thermal conduction path or heat transfer surface. We used top-side cooled GaNFETs so that we could heatsink them directly to a large copper heat spreader integral with the structure of the enclosure, to maintain the die at the lowest possible temperature. The airflow paths within the enclosure are carefully designed to have maximum thermal transfer near to the GaNFET array and for the GaNFET array to be the first cooled by incoming air. The airflow is specifically designed to avoid the CeraLink capacitor bank because these capacitors have lowest losses at or above 60°C. For this reason they are slightly insulated from the enclosure and the adjacent wall is made of thinner folded copper.

## EMC Compliance

The CZARS architecture only connects to the DC supply during a single inductor charging phase of the PWM switching cycle. During the remaining part of the switching cycle, current flows in a tight loop through the energy storage capacitor. This means that any imbalance in the inductor current does not appear as a primary PWM frequency drive source between the DC and AC connections, so that the architecture is inherently quiet even before filtering. The very high switching speed used allows the use of low valued and compact filtering inductors to attenuate residual switching noise. The large physical size of UL safety rated 'Y' capacitors needed to complete the EMI filter current path to chassis-ground proved a problem in such a small enclosure and dual redundant series connected ceramic chip capacitors were used with continuous monitoring of the series connection points such that if any 'Y' cap fails either open or short, this is immediately detected, causing a permanent shutdown logged in NV RAM. In the case of a short, the remaining series capacitor is still rated at the applied voltage, so that safety is maintained during shutdown.

## Outline of switching operation

For a zero input ripple inverter, a circuit is required which can operate in one of two modes, throughout the line frequency cycle and as required:-

- a) Supplement the input power by discharging a capacitor bank.
- b) Store excess input power by re-charging the capacitor bank.

Fulfilling operating mode a), the CZARS architecture can readily output split phase AC power at a line frequency by applying appropriate symmetrical PWM signals to the full bridge circuit and input select stage in combination, to cycle through 3 connections, such that inductor power may be i) drawn from the DC supply, ii) drawn from the energy storage capacitor, or iii) returned to

the energy storage capacitor, giving sufficient degrees of freedom, such that with appropriate control, requirement a) can be fulfilled.

Fulfilling operating mode b) is not so easy and the way that this is done constitutes the main inventive step of the IP. At first sight, it seems this circuit, with only two symmetrical inductors cannot produce an AC output whilst simultaneously transferring energy from the DC input to the storage capacitor. For example when the inverter AC output voltage is near a zero crossing with a resistive load, the inductor currents must be zero on average, but the inductors are simultaneously required to be transferring full input power from the DC input to the storage capacitor. By using a novel PWM subcarrier technique, in combination with the novel use of the output filter capacitor as temporary energy storage and making full use of the full-bridge capability to ‘flip’ the AC1 and AC2 connections, we overcome this problem. The technique involves controllably reversing the inductor current at the subcarrier frequency in synchronism with interchanging the AC1 and AC2 connections in the PWM schema, while a sub-carrier PWM ratio at the subcarrier frequency gives sufficient degrees of freedom to independently control the capacitor charge current and AC output current. The technique results in low amplitude subcarrier ripple during the charging phase, but with the output capacitor used, well below the level that would challenge the THD limit of the specification. It could of course be made lower still with a larger filter capacitor. Figure 2 shows example waveforms.

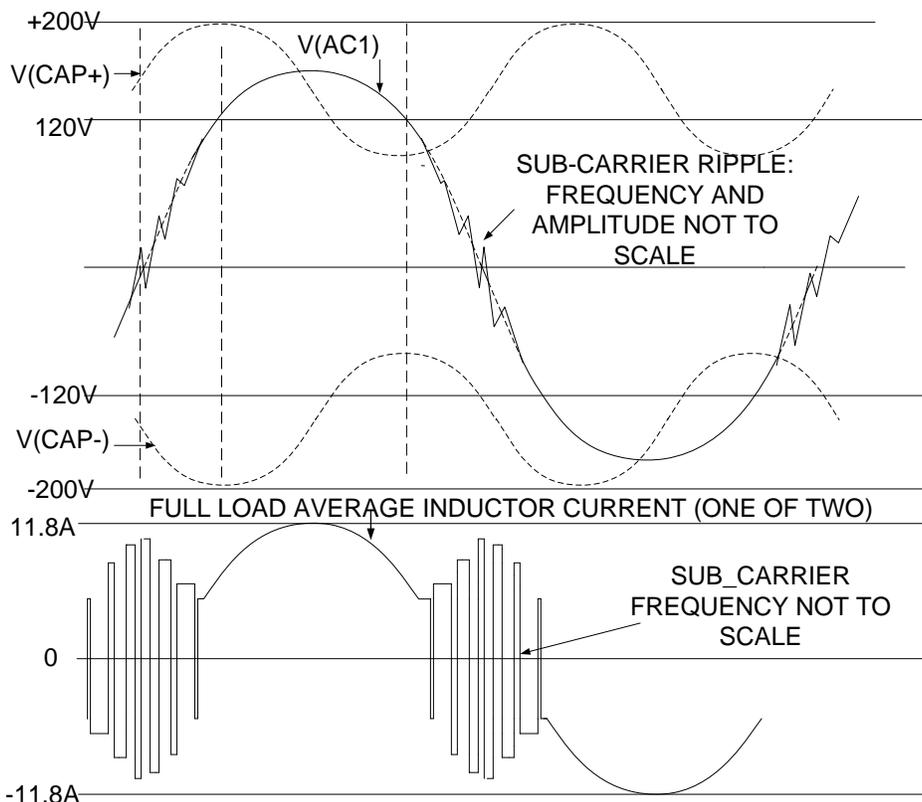


Figure 2- Voltage and current waveforms

## **Biographical Data**

### **Geoffrey P. Harvey**

CTO Adiabatic Logic,  
Project Lead

Experience: Geoff is co-founder of Adiabatic Logic and has 34 years of electronic design experience. With a knowledge of both analogue and digital electronics and been focussed most recently on the creation of high voltage mixed signal ASICs for specialist applications with an emphasis on low power.

Geoff has a particular interest in the application of adiabatic techniques to reduce power consumption and holds a number of key patents in the field. This interest and background in low energy techniques has been a key ingredient in the creation of the CZARS inverter architecture, in particular the development of a novel ZVS auxiliary switch and residual energy recovery.

Education: MA Hons Degree in Engineering, University of Cambridge, UK.

### **Stephen Love**

COO Adiabatic Logic,  
Software Lead

Experience: Steve is co-founder of the Cambridge Technology Group and has 35 years of experience in software development in real-time embedded systems.

Education: 1<sup>st</sup> Class Hons Computer Science degree London University, UK. Steve also worked at the Computer Labs, University of Cambridge, UK.

### **Dave Ruff**

Project manager

Experience: Dave has 13+ years of electronic hardware experience. Dave provides technical direction and project management.

Education: BEng 1<sup>st</sup> Class degree in Electronic and Computer Engineering University of Portsmouth, UK.