

# LBC Technical approach

**Team Name:** Energylayer

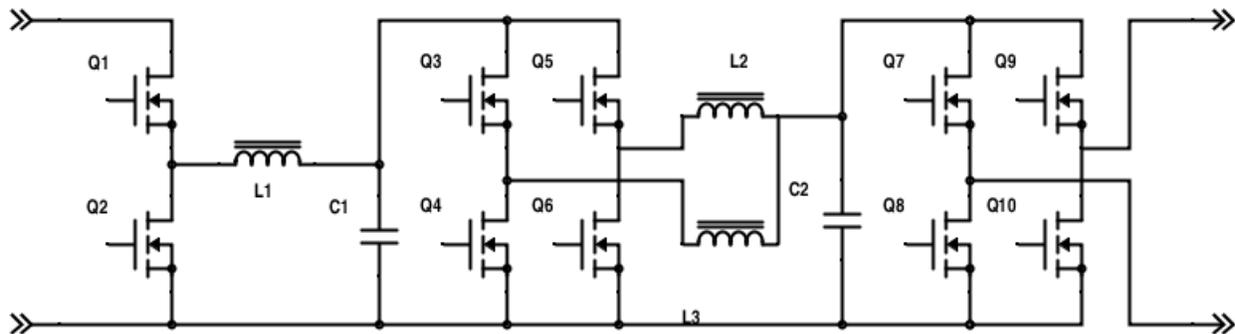
**Registration Code:** 545-fhUS03-56794

In brief, the innovations enabled us to meet and exceed contest requirements are: multi-gapped ferrite toroid inductors, high voltage/high frequency SiC switches, stacked low voltage/low frequency Si MOSFET switches, and, with less extent, using miniature low-power ARM microcontroller instead of DSP.

- **Power density achieved.**

The density of  $124.5 \text{ W/in}^3$  was achieved at a load of 2kVA resulting from enclosure dimensions of 6.9 inch x 3.7 inch x 0.63 inch.

- **Switch level schematics**



The inverter has 3 energy conversion stages:

- *buck DC-DC converter*
- *high frequency DC-DC converter* from 400Vdc to 240V, 120Hz half-sine voltage
- *low frequency DC-AC converter*

The main task of the *buck DC-DC converter* stage is to provide constant current at the output to eliminate input ripple down to  $< 2\%$ . Additionally it controls voltage on the filter capacitors not exceed 400V as an extra safety measure.

The *high frequency DC-DC convertor* form a unipolar 240V, 120Hz half-sine wave voltage. It consists of 2 identical half-bridges working in parallel in interleaved

mode such as an output current pulsated with a double frequency and a 180 degrees shift. the 2nd stage is built using SiC 900V 65 mOhm MOSFETs and fast Si freewheeling diodes. The inductors used are custom multi - gapped ferrite toroids with Litz winding.

The *low frequency DC-AC convertor* assemble a 60Hz pure sine wave AC voltage out of 120Hz unipolar pulses of 2nd stage. This stage is built using our proprietary stacked low-voltage Si MOSFET solution forming four 17 mOhm 400V switches out of 4.2mOhm, 100V silicon MOSFETs.

- **Order of magnitude passive component values**

There were electrolytic capacitors used with a capacitance of hundreds microfarads. In the DC-DC conversion stages inductors were used with the inductance values in range of tens microhenries.

- **Order of magnitude passive frequency values**

The order of frequencies are 100 to 180kHz. However due to interleaving operation the resulting current ripple at the output of DC-DC stage reaching about 360 kHz.

- **Semiconductor device types**

SiC and Si MOSFETs were employed. Please find more details below in the **Miniaturization** section.

- **120 Hz input current/voltage ripple requirement**

Although the aluminum electrolytic capacitors are considered to be undesirable component in the modern inverter they have several benefits:

- highest power density compared to film and ceramic
- no risk of unintended mechanical damage due to sub-optimal mounting like MLCC cracks
- lowest price

In our design moderate LF energy storage following the Buck stage, made by connecting in parallel a number of low-ESR ecaps. The measured overheat of such a structure is about several degrees. In terms of capacitor life it is 10-20yrs.

- **Miniaturization of components for DC/AC conversion**

- **Magnetics.** The main challenge in the DC-DC and DC-AC power conversion are inductive components. They encounter least improvements for the last several decades.

For the hundred-kilohertz switching at several thousands of Gauss the most appropriate material is the Mn-Zn ferrite. The conventional solution is the RM or more modern low profile shapes. However as the magnetic energy is stored predominantly in the air, i.e in the gaps in the magnetic path. To fully utilize this feature we use multi-gapped ferrite toroidal cores. An extra benefit of toroids is the gap(s) are shielded by the wires. Moreover as the transistors are switched in QR mode with Critical Conduction Mode the **multi-layer** inductor winding without increasing EMI is possible as inter-layer capacitance is connected in parallel to power switches' Cout and recharged at every switching cycle without significant loss and EMI.



- **Switches.** The second important component is the HV switch. We have evaluated 3 options for the high frequency PWM inverter: SiC MOSFET (Cree and Rohm), High Voltage GaN HEMTs (GaN Systems) and Low Voltage stacked GaN FETs (EPC). Ultimately we've utilized Cree 3rd Gen SiC MOSFETs, thanks to their lowest R<sub>dson</sub> thermal coefficient, low Cout and affordable price.

For the 120Hz unfolding bridge we use our proprietary custom solution: the stacked switch consisting of several low-voltage Si MOSFETs connected in series. Si MOSFETa has a "sweet spot" of FOM at about 100Vbrds

In this design 100V, 4.2mOhm devices from IR were utilized forming the 400V, 10mOhm switch.

- **Control board.** The Cortex M4 general purpose ARM microcontroller with built-in FPU was used to ensure minimal space occupied.

- **Thermal management**

Besides the forced air cooling with fans there are no extra thermal tricks employed thanks to high conversion efficiency. Moreover the special care was taken to ensure there is no direct thermal contact of any switching component to the enclosure to minimize stray capacitance for lowering EMI.

- **Electromagnetic Compliance (EMC)**

To manage EMC there are 2 approaches exist:

- mitigating electromagnetic interference in the source of generation
- proper filtering and shielding

Both were utilized in the design.

For the power transistors switching loops were minimized. Inner PCB layer was used as a combined shield and low-impedance return current path with minimal loop area.

No switching element has direct contact to the metal enclosure (i.e. do not use it as a heatsink) to minimize stray capacitance.

The quasi-resonant PWM enables ZVS in virtually all range of the loads thus lowering EMC significantly by extending voltage rise and fall times and eliminating current spikes during the transistors switching time.

The two inverter legs working in parallel in interleaved mode dramatically decreasing DM noise. It affects CM noise too as magnitudes of current are 2 times lower compared to single-leg configuration.

The input filter is pi-type CLC filter consisting of 1 Common Mode choke.

The output filter build of 2 stages consisting 1 DM and 1 CM chokes. CM choke with their stray inductance adding extra DM suppression too.

Apart the CM chokes for Common Mode filtering the feedthrough capacitors were employed to eliminate lead inductance effect in the MHz range. Also due to their good thermal conductivity it got possible to increase current density in the chokes wires to increase amount of turns.

# Biographical information appendix

## **Evgeny Sboychakov.**

[ua.linkedin.com/in/evgenysboychakov](http://ua.linkedin.com/in/evgenysboychakov)

CEO of EnergyLayer, previously worked in IT and Telecoms (Nokia Siemens Networks, Huawei, Alcatel). At NSN as a PM was working in Uzbekistan in 2009-2010 on closing a challenging full turnkey network rollout project, investment amount of ~400MM.

Being a Product manager at Huawei in 2008 was in charge of delivering 3G mobile solutions to one of the leading telecom network providers in Ukraine. Was working in a close relation with Shendzen R&D center launching several pilot projects of new mobile services.

As a field engineer in Alcatel in 2003-2005 got hands-on experience on turnkey delivery of complex technology solutions such as Radio Access Network including power supply infrastructure, data transmission networks and radio interface supporting stuff.

Has launched EnergyLayer at 2011 to bring on the market results of his own research rooted from early 2000-th studies in University of Radioelectronics on digital control of power processing and his own researches in Digitally Controlled Electrical Energy Converters, led in period of 2001 - 2010, together with experience gained in technology-reach telecom projects.

One of the latest projects developed in the power electronics domain is the design of 20kVA power supply for the Particles Accelerator; customer is Kyiv Polytechnic University.

## **Ruslan Kotelnikov.**

[ua.linkedin.com/in/rkotelnikov](https://ua.linkedin.com/in/rkotelnikov)

CTO at EnergyLayer, brings the expertise of secure enterprise Data and Web solutions. Ruslan was proven track record in several software projects gaining experience in e-commerce, banking and Internet access domains.

In 2010 at Aimprosoft he was busy on developing the internet traffic control system for the large network provider, featuring flexible quotes and users management and enabling complex reports generation. As a developer Ruslan was in charge for both backend and frontend code.

In 2011 also in Aimprosoft he developing a system of online shops monitoring aimed to analyse large amounts of data and employing complex analytics to provide a recommendation service for the customers. Ruslan was in charge for both frontend and backend development as well as further research for implementing new features.

In 2012 at BAROO software he joined a team developing SEPA payment system for the one of the leading banks. Responsible mainly for backend he developed a system for payment files processing and payments integration.

Ruslan and Evgeny meet during their work at Griddynamics in 2013 on the Macys secure webservices project. Ruslan joined Energylayer as he was impressed the perspectives of delivering low-cost programmable energy processing platform.

Ruslan is inspired with the computational algorithms, heavy math at the basis of information security and the beauty of the complex system architecture.

Besides the software development Ruslan has fundamental interest in hardware and materials areas, particularly in the Physics of Semiconductors and High-End audio amplifiers.