

## I. TECHNICAL APPROACH

In order to meet the design targets set forth by the Google Little Box Challenge, The University of Tennessee (UTK) in partnership with the Electric Power Research Institute (EPRI) has developed and implemented a new, 2 kVA single-phase inverter with ultra-high power density (**102 W/in<sup>3</sup>**). The implemented system schematic and order-of-magnitude design parameters are given in Fig. 1 and Table I, respectively. In order to achieve this power density, key developments have been made in four critical areas: 120 Hz ripple mitigation, power stage miniaturization, thermal management, and electromagnetic compliance (EMC).

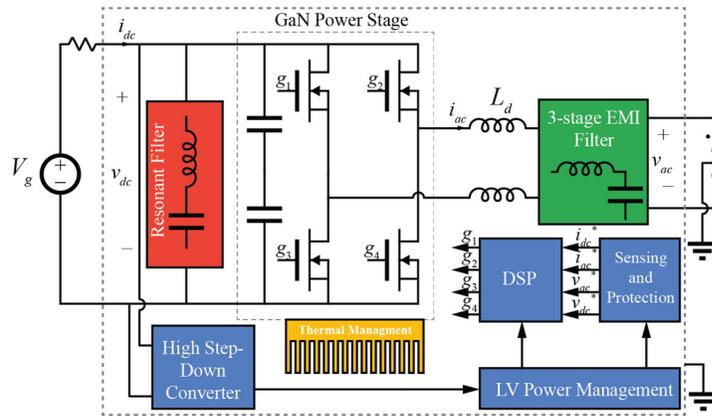


Figure 1: System schematic as implemented

TABLE I: DESIGN VALUES

Parameter	Values
Switching frequencies	100s of kHz
Semiconductor type	GaN
DC Capacitance	100s of $\mu\text{F}$
DC resonant filter inductor	< 5 mH
Enclosed Volume	19.6 in <sup>3</sup>
2 kVA power density	102 W/in <sup>3</sup>
CEC efficiency	96.9%

### 1. 120 Hz Ripple Mitigation

Traditional approaches to dealing with the instantaneous mismatch between DC power input and AC power output fall broadly into one of two categories. Passive approaches largely implement DC bulk capacitance at the inverter input which are large enough to exhibit low voltage ripple when exposed to the double line frequency ripple. However, because of the small ripple voltage and large energy stored in the DC component of the voltage, the 3% voltage ripple requirement necessitates a capacitor sized 20-fold larger than what would be used to mitigate the ripple energy at full load. Active approaches decouple the capacitor from the DC link through power electronics, allowing smaller energy storage by reducing or removing entirely the DC voltage component on the capacitor. However, the additional power electronics process as much as half of the total output power, and must process the power twice to effectively store and return the ripple energy. This approach therefore has limits in size, efficiency, and heat generation.

To meet 120 Hz ripple requirements without compromising on system size, the team has developed a new resonant DC-side filter for 120 Hz energy which reduces the volume required for storage by 65% compared to the DC-link capacitor approach, and reduces energy loss by over

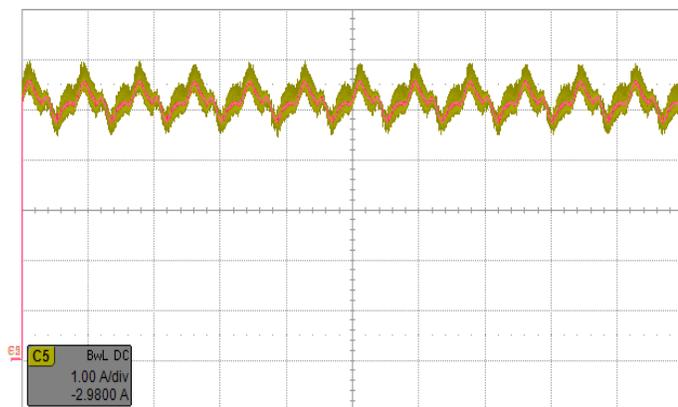


Figure 2: 2 kVA test waveform showing input current ripple of 16%. Trace F2 (pink) applies a 5 kHz low-pass filter to the raw waveform.

80% compared to the team's optimal design of an active power filter. In order to achieve this high density, the team used a custom designed, laminated supermendur core. This material was selected for its high saturation flux density and was fabricated in a geometry with maximal area-to-volume ratio.

The resonant filter performance and density have been verified experimentally as demonstrated in Fig. 2, where a 5 kHz low-pass filter is applied to attenuate switching ripple of the observed DC input current when supplying 2 kVA output power, showing just 16% ripple. The filter attenuation has been measured and verified to meet specification for the full range of load powers.

## 2. Miniaturization of the Inverter

The inverter power stage and overall system size were minimized through a multi-faceted approach. In the design stage of the project, many different approaches were analyzed through complete paper designs to compare total displacement volume. This included alternate energy storage implementations, converter topologies, switching frequencies, and device and passive materials. Complete in-house static and switching performance characterization of multiple WBG devices, including thermal variations in key parameters [1], allowed the solution to employ devices which only became available during the latter months of the competition. Thermal design volume was considered at this stage based on assumed uniform performance of a heatsink comparable to commercial products. Further details on final thermal design are given in the following section. Based on this analysis, a complete picture of the optimum solution to maximize power density was known, and a design was selected which yielded the minimum physical displacement volume while meeting all required specifications. Switching frequency was maximized to the extent that the reduction in overall volume of filter elements outweighed the additional cooling volume required because of increased switching losses.

Individual passive components were minimized through custom fabrication of capacitors and inductor cores by commercial vendors, using advanced materials. In order to maximize inductor window utilization, winding bobbins were either eliminated, or 3D printed at the Oak Ridge National Laboratory using custom-modeled designs.

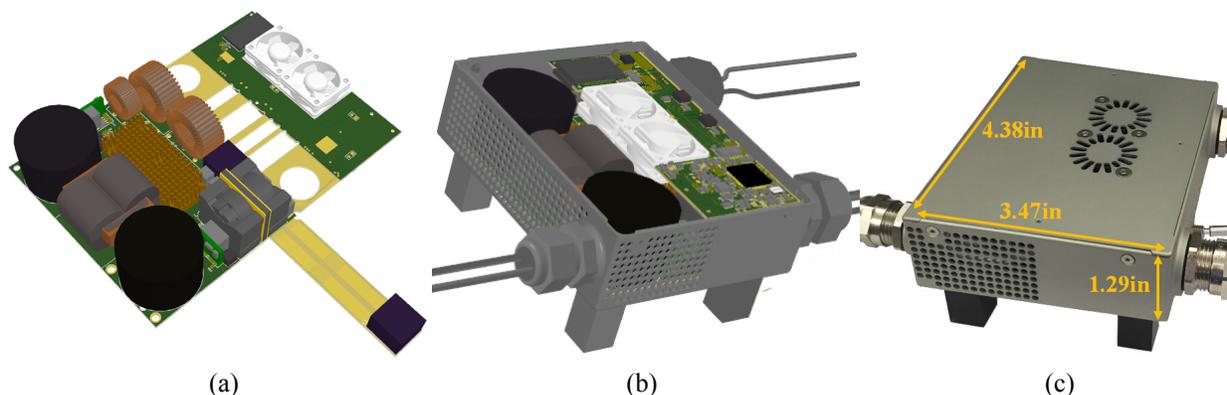


Figure 3: Rendering of PCB layout for the inverter (a) and inverter in enclosure (b); photo of final enclosed prototype system (c)

In order to achieve the present rectangular volume, which yields a power density of  $155 \text{ W/in}^3$  when unenclosed, the team iterated through more than five versions of circuit and system design, refining size and electrical performance with each design. Significant effort was put into maximizing the rectangular volume utilization; that is, optimizing the ratio of the total component

volume to the rectangular system volume. Coordination between UTK and EPRI allowed the team to continue decreasing the solution size while maintaining low electrical parasitics and meeting all thermal requirements. At present, the converter itself exhibits a volume utilization near 70%, with remaining empty volume carefully distributed as necessary for adequate cooling. The final design mockup used in thermal analysis and in fabrication is shown in Fig. 3. A printed circuit board with flexible interconnect cabling is used to allow control, low voltage power conversion, and protection circuitry to reside on the top side of the enclosure, providing additional shielding for sensitive circuitry and utilizing otherwise open space in the enclosure. Each dimension of the enclosure has been reduced to the minimum possible with the components in the design.

### 3. Thermal Management

Through a collaborative arrangement between UTK and EPRI, the team gained expertise in 3D finite-element thermal analysis. Leveraging this capability, the team worked together to simulate and modify circuit layout, component placement, enclosure and heatsink design, and fan selection with each subsequent revision. This closed-loop approach allowed the team to design a thermal management system which removes heat from the box greater than 50% heat-to-air transference ratio (the typical limit for laminar flow-dominated systems).

To push the power density limits in a rectangular enclosure, the team iterated back-and-forth between altering enclosure, heatsink, and fan design and altering component design and placement to force the design to its thermal limits while meeting the required external temperature specification. Full 3D FEA models using analytical loss models for each component, and eventually verified losses from benchtop experimental tests were used to carefully route airflows to provide maximum cooling while still allowing sufficient distance for the air to mix and exit the box below the competition's temperature limits.

An example of the iterative FEA process is given in Fig. 4. In Fig. 4(a), an initial thermal design based on finned heatsink and series intake and outflow fans was used. A combination of non-optimized component placement, flow management, and distance given for mixing of air, resulted in surface temperatures above 60°C. In Fig. 4(b), components and grilles are rearranged and a new, custom pin fin heatsink with conformal thermal interface and graphite heat spreader is used to improve heat transfer, direct airflow to the hottest components, then leave sufficient time for mixing so that the air temperature leaving the box is below the limit. In Fig. 4(c), the redesigned system's enclosure temperature is verified to meet the requirements with a maximum enclosure surface temperature of 52°C with a 2 kW load.

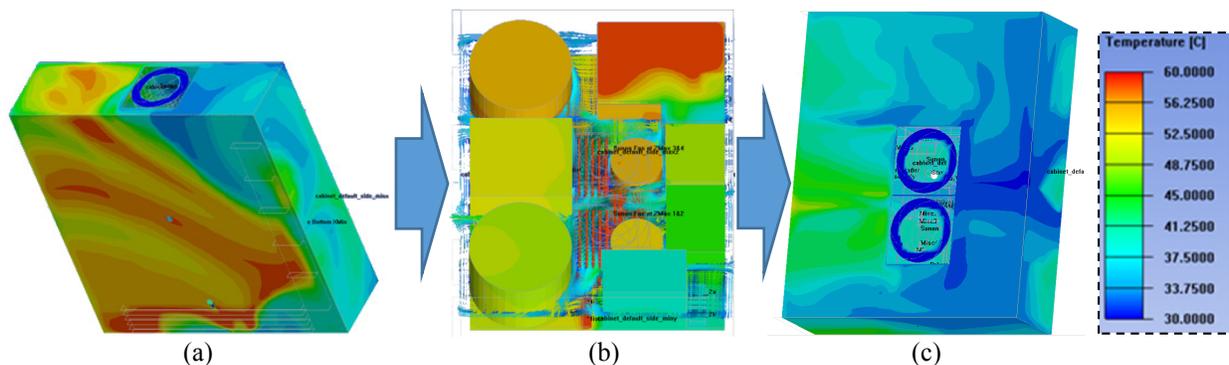


Figure 4: Iterative FEA-based thermal design. In (a) a traditional approach yielded enclosure temperatures above specification. Air flows and heat distribution are analyzed in (b) to yield a new thermal design which meets specification (c). All figures share a common scale, at right.

#### 4. Electromagnetic Compliance

Because of the difficulty in meeting the EMI specification in a restricted volume, the team has allocated space within the enclosure for a high density, three-stage filter at the AC output. The filter includes a two-stage symmetrical differential mode (DM) LC-filter using a combination of ferrite and powder-core materials, and optimized winding and core geometry to maximize achievable attenuation in a minimal volume, subject to thermal constraints. A pair of nanocrystalline common-mode (CM) chokes are used for high density. In the present prototype, the CM capacitance is limited by the original 5 mA leakage requirement; with the updated specification, the team has headroom to increase the performance of the CM filter, obtaining additional attenuation beyond the requirements in advance of the October testing. This approach limits leakage current at the switching frequency (100s of kHz), beyond the 0-50 kHz measurement specified.

The DM capacitances are limited due to the nature of the DC resonant filter used to meet input DC ripple requirements. DC filter attenuation degrades minimally with leading power factor. In order to ensure less than 20% current ripple at 0.7 load power factor, a maximum of just under 6.6  $\mu\text{F}$  DM capacitance can be employed. To ensure sufficient margin, 3.3  $\mu\text{F}$  capacitors are used, resulting in a DC ripple which remains 20% below the limit at 0.7 leading power factor. The resulting DC ripple across varying power factors is shown in Fig. 5(a), relative to the specified limit.

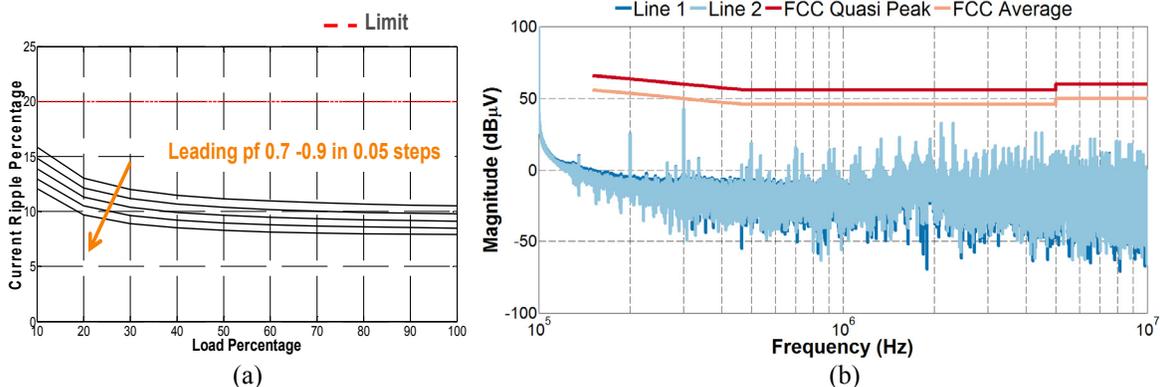


Figure 5: (a) analytical input current ripple with 3.3 $\mu\text{F}$  DM capacitance; (b) simulated noise for the design. Note that both show performance meeting specifications

Fig. 5(b) shows EMI simulations of DM and CM noise for the current system, demonstrating that both meet the required standard.

The testing application submitted jointly with this document shows the results of the team's efforts in the four key areas outline here. The system is fully functional and capable of meeting all required specifications with a power density of **102 W/in<sup>3</sup>**.

- [1] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, B. Liu, and R. Ren, "Characterization of an Enhancement-Mode 650-V GaN HFET," *IEEE Energy Conversion Congress and Exposition (ECCE)* 2015, pp.400-407, 20-24 Sept. 2015

## II. Biographical Information

This team consists of members from the University of Tennessee Knoxville (UTK) and the Electric Power Research Institute (EPRI), with significant contributions from Oak Ridge National Laboratory (ORNL).

### The University of Tennessee Knoxville

**Daniel Costinett** received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Colorado, Boulder, concluding in 2013. In 2012, he assisted with research and course development as an instructor at Utah State University. He is currently an Assistant Professor in the Department of Electrical Engineering and Computer Science at the University of Tennessee, Knoxville. His research interests include resonant and soft switching power converter design, high efficiency power supplies, mixed-signal integrated circuit design, medical devices, and electric vehicles. Dr. Costinett is the Co-Director of Education and Diversity for the National Science Foundation/Department of Energy Research Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT). He is also a Joint Faculty with the Power Electronics and Electric Machinery Research Group, Oak Ridge National Laboratory. He currently serves as Associate Editor for IEEE Transactions on Industry Applications.

**Leon Tolbert** received his B.S., M.S., and Ph.D. in electrical engineering from the Georgia Institute of Technology. He worked at Oak Ridge National Laboratory (ORNL) in Oak Ridge, Tennessee, from 1991 to 1999. He then joined The University of Tennessee, Knoxville, where he is presently the Min H. Kao Professor and Department Head in Electrical Engineering and Computer Science. He is also a part-time senior research and development engineer with the Power Electronics and Electric Machines Group at ORNL. His research interests include gate drives and high temperature packaging of power electronics, application of wide bandgap (SiC and GaN) power electronic devices, electric vehicles, and utility interface with renewable energy and microgrids. He is a Fellow of the IEEE and a registered Professional Engineer in the state of Tennessee.

**Fei (Fred) Wang** received his Ph.D. degree in electrical engineering from University of Southern California (USC). He was a Research Scientist in the USC Electric Power Lab from 1990 to 1992. He joined the GE Power Systems Engineering Department, Schenectady, NY, as an Application Engineer in 1992. From 1994 to 2000, he was a Senior Design Engineer with GE Industrial Systems, Salem, VA. During 2000 to 2001, he was the Manager of Electrical Systems Technologies Lab, GE Global Research Center, Niskayuna, NY and Shanghai, China. From 2001 to 2009, he was an Associate Professor at the Center for Power Electronics Systems (CPES), Virginia Tech. Since 2009, he has been with The University of Tennessee, Knoxville (UTK) and Oak Ridge National Lab as a Professor and Condra Chair of Excellence in Power Electronics. He is a founding member and Technical Director of the NSF/DOE Engineering Research Center CURENT at UTK.

**Chongwen Zhao** received the B.Sc. degree from the School of Electronic Engineering, Xidian University, Xi'an, China, in 2011, and received the M.Sc. degree from the College of

Electrical Engineering, Zhejiang University, Hangzhou, China, in 2014. Currently, he is working toward the Ph.D. degree in electrical engineering at the University of Tennessee, Knoxville, TN, USA. His research interest includes wireless power and communication applications, DC-DC power conversion.

**Bradford Trento** received the B.S and M.S. degrees in electrical engineering from the University of Tennessee, Knoxville. Mr. Trento is the Industry Liaison for the Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT) an NSF engineering research center. Before joining CURENT, Mr. Trento worked at the Electric Power Research Institute (EPRI) as an engineer in the Critical Power Program from 2007-2012. His research interests include modeling and control of grid-tied converters.

**Ling Jiang** received her B.S. degree in thermal energy and power engineering from the Nanjing University of Science and Technology, Nanjing, China in 2007. She received the M.S. degree in electrical engineering from Tongji University, Shanghai, China in 2011. She worked as an electrical engineer in Global Development Center in Philips in Shanghai from 2011 to 2014. Currently, she is a PhD student in the Department of Electrical Engineering and Computer Science at the University of Tennessee, Knoxville. Her research interests include resonant and soft switching high power density power converter design.

**Bo Liu** received his B.S. degree and M.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China in 2009 and 2012. He is currently working toward the Ph.D. degree in electrical engineering at the Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT), The University of Tennessee, Knoxville. His research interests include control of power converters, hybrid ac/dc transmission system, grid emulation device, ac/dc PFC and EMI filter design.

**Zheyu Zhang** received the B.S. and M.S. degrees from Huazhong University of Science and Technology, Wuhan, China, and Ph.D. degrees from The University of Tennessee, Knoxville, TN, in 2008, 2011, and 2015, respectively, all in electrical engineering. He is currently a research assistant professor in Electrical Engineering and Computer Science, The University of Tennessee. His research interests include wide band-gap semiconductors and application, gate driver technology, motor drive design, operation, integration and reliability.

#### The Electric Power Research Institute, Inc.

**Rick Langley** received the M.Sc. degree in electrical engineering from Clemson University, in 1997. Since then, Mr. Langley has been with the Electric Power Research Institute (EPRI) and is currently the Program Manager for EPRI's Critical Power Program (CPP). The CPP supports EPRI R&D programs as well as federal programs and offices responsible for national defense, intelligence, and security. The CPP provides a wide range of science, engineering, and consulting services that includes electric power systems modeling, engineering design, evaluation and testing, design-build-test of hybrid power systems, critical load protection, power conditioning and backup power systems using a blend of custom, MOTS, and COTS hardware and software solutions.

**John F. Jansen** is presently a senior staff member at the Electric Power Research Institute (EPRI), Knoxville, TN. Dr. Jansen received the B.S. (1977) and M.S. (1979) degrees in Electrical Engineering at University of Florida; and the Ph.D. in Electrical Engineering at

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**Reid Kress** is a Senior Technical Leader at the Electric Power Research Institute (EPRI), Knoxville, TN. He holds a BS (80) and MS (82) in Mechanical Engineering from the University of Tennessee (UT) and a PhD from the University of Arizona in Mechanical Engineering with a minor in Electrical Engineering. His primary focus is in finite element analysis of multi-physics systems, specifically thermal, fluids, and electromagnetics principally applied to high-performance system design; for example, robotics, critical power applications, and mechatronics. Prior to joining EPRI, Reid was a Senior Technical Advisor for the Department of Energy's Y-12 National Security Complex (2003-2014), an Assistant Professor in the Mechanical Engineering Department at UT (2000-2003), and a Group Leader in the Robotics Division of Oak Ridge National Laboratory (1987-2000). Reid has three US Patents, teaches in the Industrial Engineering Department of UT, and is a licensed professional engineer.

**Anthony A. Brun** is a Senior Mechanical Designer who provides Design Consultation and Computer Aided Drafting for various high-tech companies in the Knoxville Oak Ridge area. He holds a BS (98) in Mechanical Engineering from the University of Tennessee Knoxville. His primary focus is assisting start-ups develop new products and devices to expedite bringing them to market. Previous employment were the design and implementation of all aspects of next generation Proton Therapy equipment for cancer treatment at Pronova Solutions. (2012-2013), Department Head of Mechanical Engineering for high-speed automated sewing equipment for Tice Engineering (1999-2001), Senior Mechanical Design Engineer for various Medical Imaging (PET) Scanners with CTI PET Systems (1987-1999). Major projects have included design of very first of its kind combined PET & CT Medical Imaging Scanner, and numerous packaging methods to detect Radiation for Homeland Security. Specializes in fast-paced mechanical design/packaging and in quick-turn fabricating to build first prototype.