Team Name: Fraunhofer IISB	Registration Code: 545-jQnRVL-59814

Abstract

The Fraunhofer IISB approach resulting in a power density of **201 W/inch³** (86.5 mm x 75.5 mm x 25 mm = 0.163 dm³ @ 2kW) is based on a 6-switch power topology with latest SiC MOSFETS from Cree. With the 6-switch approach not only the 120 Hz input ripple requirements can be fulfilled with the smallest possible energy storage but also extreme low chassis/PE ground current requirements, as originally specified, can be fulfilled.

6-switch topology approach

Fig. 1 shows the used topology based on the latest 900 V SiC MOSEFTs from Cree.

DC input requirements

Inverters with high DC input requirements, what means low input voltage as well as low input current ripples would need a very large DC-link capacitor by using a conventional design. The required energy W_{store} which has to be stored during one AC period is defined by: the maximum AC output power P_{max}, the AC frequency f_{AC} and the efficiency η. It can be calculated by:

$$W_{store} = \frac{P_{max}}{2\pi f_{AC}\eta} \quad (1)$$

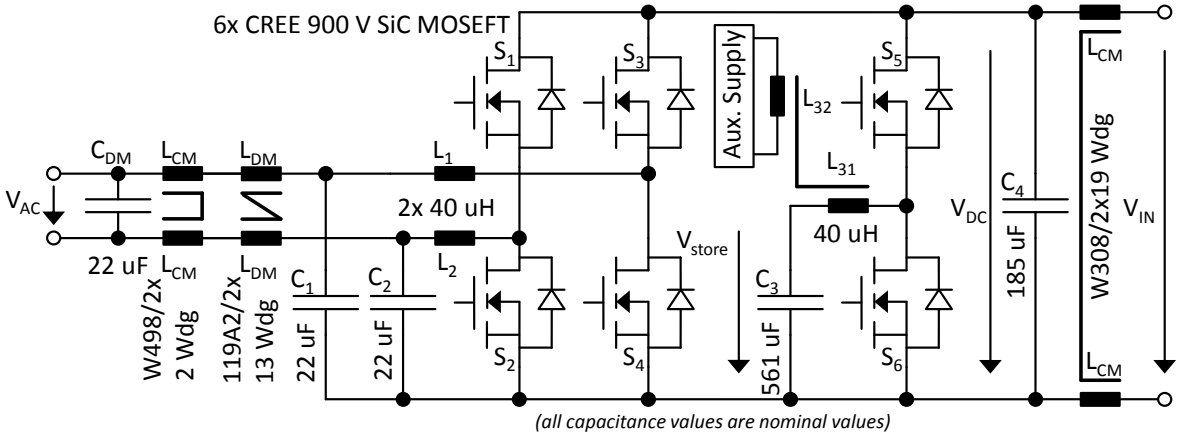

Fig. 1: 6-switch topology proposed by Fraunhofer IISB

Switches S_1/S_2 together with L_2 as well as switches S_3/S_4 together with L_1 can be used to produce a sinusoidal output voltage V_{AC} by pulse width modulation at a fixed switching frequency of 140 kHz. By choosing via software the balanced control mode, producing two sinusoidal 60 Hz waveforms with a DC-offset equal to half the DC-link voltage V_{DC}, also a maximum chassis/PE ground current of less than 5 mA, while having a high parasitic capacitance between the DC-side and ground, can be fulfilled in a split-phase load configuration. In applications with lower ground current requirements (e.g. <50 mA) the more efficient unbalanced operation mode can be used in which each half bridge is generating either the positive or the negative 60 Hz half wave.

With: P_{max}=2 kW, f_{AC}=60 Hz, η=0.97 W_{store} is equal to 5.47 J. With (2) the minimum required input capacitance C_{min} for a given energy W_{store} and a maximum voltage swing, given by values V_{Cmin}, V_{Cmax}, can be calculated:

$$C_{min} = \frac{2W_{store}}{V_{Cmax}^2 - V_{Cmin}^2} \qquad (2)$$

By using a conventional design (V_{Cmax}≈406 V, V_{Cmin}≈394 V) C_{min} is equal to 1.14 mF with an RMS current of ca. 3.5 A. Thus e.g. three 390 uF electrolytic capacitors with 450 V voltage rating in a rectangular volume of ca. 3x(0.3x0.3x0.4)dm³=0.1 dm³ would be necessary, which would be more than half of the Fraunhofer IISB Little Box solution. With the 6-switch approach switches S_5/S_6 together with L_{31} can be used to allow a much higher voltage swing on energy storage C_3. E.g. with: V_{Cmax}=380V, V_{Cmin}=190 V, C_{min} equals ca. 100 uF, what means a reduction of the necessary input capacitance value of **more than a factor of 10**. By using tiny rectangular shaped capacitors the available volume can be perfectly filled.

Miniaturization of components

The function of the Little Box is to convert a DC voltage in a pure 60 Hz AC sine wave. To fulfill this task power electronic as well as auxiliary electronic circuits are necessary. The power electronic circuit parts can be classified into active devices like power transistors and diodes and passive devices like coils, capacitors or EMC devices. Due to the littleness of the active parts compared with the passive parts the overall volume of the Little Box is defined mostly by the passive devices and the auxiliary circuits like control, gate drive and supply circuits, cooler parts and fans. By using higher switching frequencies the volume of the passive power electronic parts can be minimized of course. But to achieve the smallest possible overall volume of the Little Box a very well defined compromise between switching frequency, switching speed, switching and conduction losses and cooling effort must be found. The Fraunhofer IISB solution hence uses the latest 900 V SiC MOSFETs from Cree operated at a high switching frequency of 140 kHz but below the conducted EMC measurement standard of 150 kHz. With this approach the maximum efficiency point is designed at ca. 1.5 kW according to the most important efficiency weighting factor. Besides the usage of the latest power transistors, the most suitable power electronic topology is extreme important. As described above allows the proposed 6-switch topology a reduction of the capacitance value of the 120 Hz AC ripple storage capacitor by a factor of more than 10. Moreover, by using the necessary half bridge with power coil and gate drive additionally (and together with auxiliary winding L_{32}) as an auxiliary power supply circuit the overall volume of the Fraunhofer IISB Little Box gets optimized.

Thermal management

The thermal management of the Little Box is direct associated with the achieved efficiency. Two different general approaches can lead to the smallest overall volume. The

first one is based on a very high efficiency in the range of 99% and above, thus a passive cooling technique would be sufficient to achieve the target of a maximum surface temperature of less than 60°C. The second one is based on a still high efficiency in the range of 97% together with a forced air cooling. Because the passive parts are dominating the overall volume as well as the efficiency of the Little Box, the Fraunhofer IISB uses the second one – the forced air cooling approach. A verification of the thermal management is done by simulations as well by measurements. Fig. 2 shows for example the result of an air flow simulation.

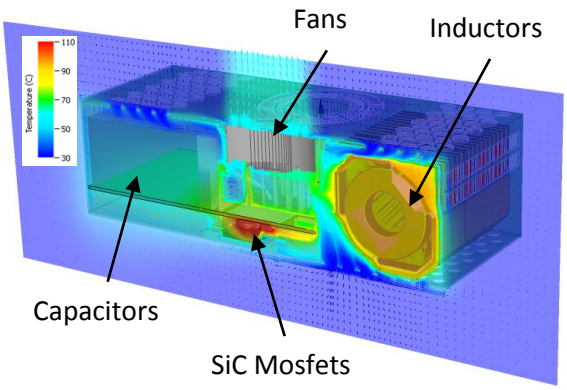

Fig. 2: Air flow Simulation of the Fraunhofer IISB Little Box solution

With an efficiency of 96.7% at 2 kW output power approx. 68 W losses P_{loss} must be taken into account. The necessary air flow rate Q_{air} is given by:

$$Q_{air} = \frac{P_{loss}}{c_p \Delta T \rho} \quad (3)$$

With a specific heat capacity c_p for air of about 1005 $Jkg^{-1}K^{-1}$, a minimum temperature difference ΔT of 30 K and the density ρ for air with 1.164 kgm^{-3} a minimum air flow rate of approx. 2 liter per second can be calculated. To achieve this air flow rate, the Fraunhofer IISB approach uses three tiny fans.

Harmonics, ground currents and EMC

While processing the AC output power different standards must be taken into account. They can be separated into very low and low frequency requirements like maximal ground currents and higher harmonics levels and high and very frequency requirements like maximal allowed conducted and radiated EMC levels. By using a switching frequency of 140 kHz the first frequency, which have to be considered for conducted EMI, is 280 kHz. With the shown forth-order low-pass filter a high noise damping level at 280 kHz of about 110 dB can be achieved. To reduce the effort for suppressing common mode currents the internal cooler is connected to $-V_{DC}$, hence no Y-capacitors are necessary. Thus the limits for FCC Part 15 B compliance can be fulfilled with two additional common mode chokes on the DC-input and the AC-output. Due to the high switching frequency of 140 kHz the very high, high and low frequency requirements (higher harmonics of 60 Hz) can be fulfilled with small passive components. Whereas, special attention needs the most critical, very low frequency (60 Hz) requirement of a very low chassis/ground current (e.g. < 5mA) in applications with a high parasitic capacitance C_{par} between the DC-input and ground (PE). Fig. 3 illustrates the problem.

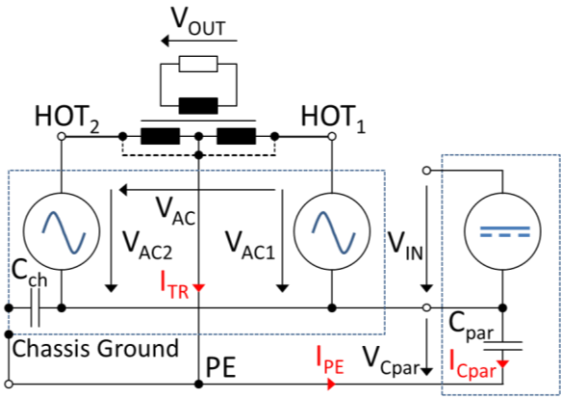

Fig. 3: 60 Hz ground current problem

If the parasitic capacitance C_{ch} is much smaller than C_{par} additional currents via the chassis can be neglected, thus: $I_{PE}=I_{TR}=-I_{Cpar}$. With the proposed topology shown in Fig. 1 and an asymmetrical output configuration (as illustrated by dotted lines in Fig. 3) at least half of the AC amplitude voltage is across C_{par}. With C_{par}=200 nF, f_{AC}=60 Hz, V_{Cpar}=120 V_{rms} and the following equation:

$$I_{PE} = -I_{Cpar} = 2\pi f_{AC} C_{par} V_{Cpar} \qquad (4)$$

I_{PE} equals at least 9 mA. The Fraunhofer IISB approach uses a symmetric (split phase) configuration. Hence, via software, the balanced operation mode can be activated. In this mode V_{Cpar} equals theoretical zero, thus I_{PE} would be zero. In applications with lower ground current requirements (e.g. I_{PE}<50 mA) the Fraunhofer IISB approach allows to use the unbalanced operation mode with an increased efficiency of the Little Box. In Table 1 the RMS voltage between DC- and ground as well the ground current I_{PE} is given for different power circuit topologies, output configurations and operation modes at a glance.

Table 1 shows that the Fraunhofer IISB approach can also fulfill the original Little Box specification. Moreover, Table 1 shows that using a totem pole topology, which requires only one power coil, is not preferable. With a power factor of +/- 0.7 and 200 nF maximum parasitic capacitance between DC- and PE, the AC current commutating via the freewheeling body diode during zero voltage crossing is up to ca. 8 A. In this case the dV/dt-level at C_{par} is much higher as calculated in Table 1, resulting in a ground current above 50 mA_{rms}.

Table 1: 60 Hz ground currents for different topologies for C_{par} = 200nF (120nF) and 60 Hz RMS voltage between DC- and ground (grey lines: Fraunhofer IISB solution)

Description of power topology	Description of the wave form of V_{Cpar}; **$V(DC-,PE)_{RMS}$**	I_{PE} (mA_{rms})
totem pole [1]	Trapeze (0V/-V_{DC}V) with t_r=t_f=0.33ms e.g.; **max. 318 V_{rms}** @ DC = 450 V (light load)	48.1 (28.9)
asym. config. & unbalanced	-340V*abs(sin(2πft)) for one half wave other half wave zero; **170 V_{rms}**	12.8 (7.7)
sym. config. [2] & unbalanced	-170V*abs(sin(2πft)); **120 V_{rms}**	9.1 (5.4)
asym. config. & balanced mode	170V*sin(2πft)-200V; **233 V_{rms}**	9.1 (5.4)
sym. config. [2] & balanced mode	-V_{DC}/2 = const. = -200V; **200 V_{rms}**	0 (0)
60 Hz sine with one half bridge & asym. config. & coded plug [3]	-V_{DCfull}/2 = const. 350V (e.g.) **350 V_{rms}**	0 (0)

[1] Only for resistive loads (with reactive loads t_r/t_f are load dependent)
[2] Not possible in all countries (split phase config. necessary)
[3] Not possible in all countries (coded AC-plug necessary)

Biographical information appendix

First one: team's point of contact, afterwards in alphabetical order:

Dr.-Ing. Bernd Eckardt (1977), studied electrical engineering at the Friedrich Alexander University Erlangen (FAU) focused on analog circuit design. After the Diploma Degree 2003, he joined the Fraunhofer IISB working on automotive DC/DC converter systems. In 2007 he became head of the group "System Integration". In his Ph. D. studies, finished in 2010, he also focused on very high power density DC/DC converters and there application in automotive powertrains. Since 2014 he is head of the "Vehicle Electronics" department working on highly efficient and compact power electronic systems, with high switching frequencies, wide bandgap semiconductors (SiC, GaN), improved EMI and deep mechatronic integration.

Dipl.-Ing. Stefan Endres (1985), received the Dipl.-Ing. degree in Mechatronics from the Friedrich-Alexander-University of Erlangen-Nuremberg, Germany, in 2011. From 2012 until 2013 he was working for the Friedrich-Alexander-University of Erlangen-Nuremberg, Chair of Electron Devices. Since January 2014 he is employed at the Fraunhofer IISB. His main topic is developing hardware and software for microcontroller based highly integrated and modularized power converters.

Dr.-Ing. Maximilian Hofmann (1981), has studied mechanical engineering at the Friedrich Alexander University Erlangen. He is head of the group 'Drives and Mechatronics' in the department 'Vehicle Power Electronics' at Fraunhofer IISB. His main R&D focuses are inverter power electronics for electric drives, power stages for highest switching frequencies and power densities and the mechatronic integration of electronics in harsh environments.

Dipl. Ing. Stefan Matlok (1985), studied mechatronics at the Friedrich Alexander University Erlangen majoring power electronics. Since 2011, he specialized for switching circuit designs and develops FPGA and µC control boards for high power traction converters. As head of the DC/DC converter group at the Fraunhofer IISB, he works on new prospects improving functional features, EMI, efficiency and loop stability by using digital control techniques.

Dipl. Ing. Thomas Menrath (1985), studied mechatronics at the Friedrich Alexander University Erlangen. Since 2013 he works for the DC/DC converter group at Fraunhofer IISB. His main field of research is design and simulation of liquid and air cooling systems for electronic devices with restricted space.

Prof. Dr.-Ing. Martin März (1962), studied electrical engineering at the University of Erlangen-Nuremberg specializing in high frequency engineering. After his PhD on laser topics, he started his career in the semiconductor division of the Siemens AG, later Infineon AG. Since 2000 he is working for the Fraunhofer "Institute of Integrated Systems and Device Technology" in Erlangen and Nuremberg (Germany) as head of the power electronics system department, since 2012 as the deputy director of the IISB. He is working on system integration of power electronics, thermal management, and on new technologies for power density, efficiency, and reliability improvements.

Dr.-Ing. Stefan Zeltner (1969), has completed a four year apprenticeship in electronics in 1989. After a short period in industrial R&D labs he has studied communications engineering at the Georg Simon Ohm University of applied sciences Nuremberg and electrical engineering at the Friedrich Alexander University Erlangen-Nuremberg. Since 2001 he is a research associate of the power electronics division at the Fraunhofer Institute for Integrated Systems and Device Technology IISB. Since 2007 he is head of the AC/DC converters development group. In 2011 he finished his PhD in the field of insulating low loss gate drivers. His research interest is focused on modular high power density electronics.